IPVTADC6BIT65

6-bit 8GS/s TADC

Product Brief

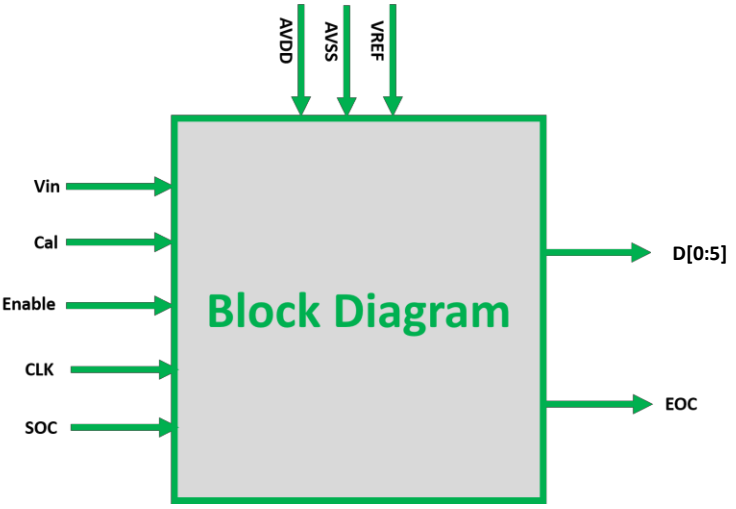
Features

- TSMC 65nm General Purpose Process (G)
- 1.0 V Single Supply Voltage
- 6-bit Time-Interleaved Time-Based ADC
- 8GS/s Maximum Sampling Rate (Fs)
- Input Clock CLK= (1/8) x Fs
- Input Signal Range: 0.9 Vpp
- Input Signal Common-Mode: $V_{DD}/2$
- Outstanding Static Performance:
  - DNL = ± 0.5LSB
  - INL = ± 1.0LSB
- Outstanding Dynamic Performance:
  - 35.2 dB SNDR at fin = 1GHz
  - 5.7-bit ENOB at fin = 1GHz
- Low Power Dissipation:
  - 328 mW at Fs = 8GS/s
  - 33.5 mW at Fs = 1GS/s
- Compact Die Area: Only 4.24 mm^2

Applications

- High Speed Acquisition
- Software Defined Radio Prototyping
- 3G/4G Radio Receivers

Block Diagram



Block Description

The IPVTADC6BIT65 is a low-power 6-bit Time-Interleaved Time Based ADC IP with a sampling rate up to 8GS/s. The TADC uses converts the analog signal to Pulse Width Modulation (PWM) signal and then digitize the PWM signal to a 6-bit digital word.

Considering a sampling rate of 8GS/s, a 1GHz input frequency and an input range of 0.9Vpp, this 6-bit ADC features an outstanding dynamic performance that includes 35.2 dB SNDR and 5.7-bit ENOB.

The power dissipation of this ADC scales linearly with the sampling rate. At 8GS/s and 1GS/s, the ADC dissipates 328mW and 33.5mW, respectively.

Upon request, the IPVTADC6BIT65 can be cost-effectively ported across process nodes and different foundries.

IP Deliverables

- Datasheet
- Layout View (gds2)
- Integration Support

IP at IP VALLEY

IP VALLEY provides various Mixed Signal IPs. The Mixed Signal IP includes high performance ADC and DAC convertors, Power Management, Clocking Circuits, and other IP building blocks

IP VALLEY IP cores have been silicon verified in a number of foundries (TSMC, Global Foundries, UMC, and Fujitsu) at nodes ranging from 180nm to 45nm.