IPVLPIOTRAES30

0.2mW 30Mbps IoT Reconfigurable AES

Product Brief

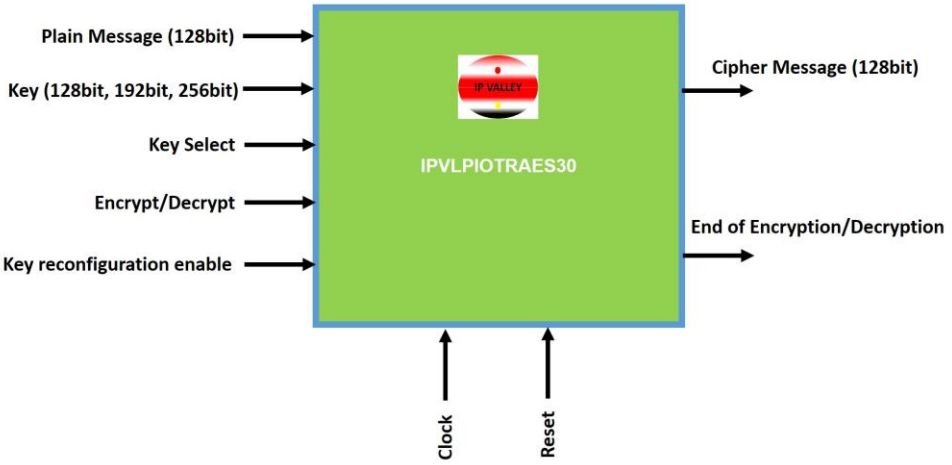
Features

- Implements AES (Rijndael) to latest NIST FIPS PUB 197
- 0.2mW maximum power consumption
- Maximum throughput of 30Mbps
- Reconfigurable AES key (128bit, 192bit, and 256bit)
- Handles encryption/decryption and key expansion in one IP core
- Supports all AES operating modes.
- Optimized for Xilinx FPGA kits
-

Applications

- Low power tiny area IoT hardware security modules

Block Diagram



Block Description

The IPVLPIOTRAES30 soft IP is intended to be used in Xilinx FPGA kits as an RTL optimized code. In addition, it is available as a hard ASIC IP which can be cost-effectively ported across process nodes and technology foundries.

The hard ASIC IP provides up to 30Mbps throughput with power consumption of 0.2mW and very small Silicon area.

IP Deliverables

- Datasheet
- RTL code for the soft IP core
- Layout View (gds2) for the hard ASIC IP core
- Integration Support

IP at IP VALLEY

IP VALLEY provides various Digital IPs. The Digital IP (hard, generic, and soft IPs) includes IoT security hardware modules, Communication blocks supporting LTE and 5G, Biomedical processing IPs for neural EEG signal processing, and Compression IP cores.

IP VALLEY Digital hard IP cores have been silicon verified in a number of foundries (TSMC, Global Foundries, UMC, and Fujitsu) at nodes ranging from 180nm to 22nm.