IPVADC10BIT130

10-bit 30MS/s SAR ADC

Product Brief

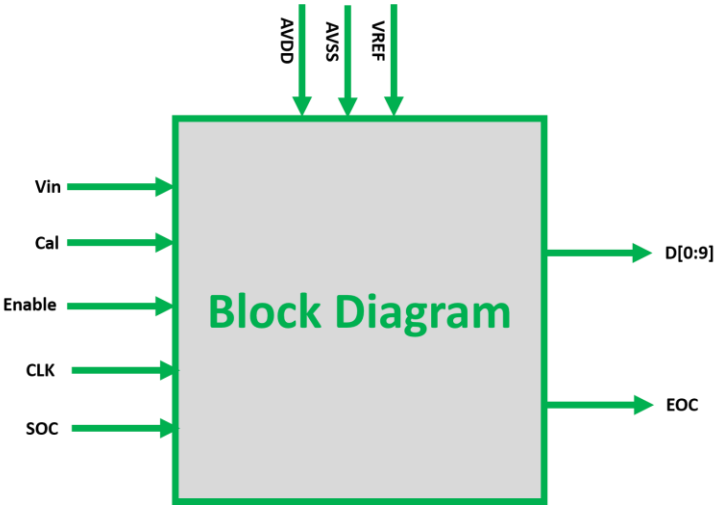
Features

- UMC 0.13um General Purpose Process (G)
- 1.0 V Single Supply Voltage
- 10-bit SAR ADC
- 30MS/s Maximum Sampling Rate (Fs)
- Input Clock CLK= 16 x Fs
- Input Signal Range: 1.0 Vpp
- Input Signal Common-Mode: VDD/2
- Outstanding Static Performance:
  - DNL = ± 0.5LSB
  - INL = ± 1.0LSB
- Outstanding Dynamic Performance:
  - 59dB SNDR at fin = 1MHz
  - 9.5-bit ENOB at fin = 1MHz
- Very Low Power Dissipation:
  - 2.8 mW at Fs = 30MS/s
  - 125 uW at Fs = 1MS/
- Ultra Compact Die Area: Only 0.09 mm^2

Applications

- General Purpose Acquisition
- Power Management
- Monitor Applications

Block Diagram



Block Description

The IPVADC10BIT130 is a low-power 10-bit Successive Approximation Register (SAR) ADC IP with a sampling rate up to 30MS/s. The SAR algorithm uses a new SAR algorithm that depends on our novel continuous dis-assembly algorithm.

Considering a sampling rate of 30MS/s, a 1MHz input frequency and an input range of 1.0Vpp, this 10-bit ADC features an outstanding dynamic performance that includes 59 dB SNDR and 9.5-bit ENOB.

The power dissipation of this ADC scales linearly with the sampling rate. At 30MS/s and 1MS/s, the ADC dissipates 2.8mW and 0.125mW, respectively.

Upon request, the IPVADC10BIT130 can be cost-effectively ported across process nodes and different foundries.

IP Deliverables

- Datasheet
- Layout View (gds2)
- Integration Support

IP at IP VALLEY

IP VALLEY provides various Mixed Signal IPs. The Mixed Signal IP includes high performance ADC and DAC convertors, Power Management, Clocking Circuits, and other IP building blocks

IP VALLEY IP cores have been silicon verified in a number of foundries (TSMC, Global Foundries, UMC, and Fujitsu) at nodes ranging from 180nm to 45nm.